Remarks

Claims 1-14 are pending in the application. It is noticed that the Office Action Summary mentions claims 1-13 only, whereas the Detailed Action duly addresses all claims 1 through 14. It is therefore considered that mention of claims 1-13 instead of claims 1-14 in the Office Action Summary is due to a typographical error.

Claims 1-5 and 7-14 are rejected.

Claim 6 is objected to.

Allowable Claims

The Applicants thank the Examiner for the indication that Claim 6 would be allowable if rewritten to incorporate the elements of claim 1. However, because the Applicant believes that the remaining claims in this application are patentable, the Applicant has not rewritten Claim 6 in independent form.

Rejection under 35 U.S.C. § 102

The Office Action rejects Claims 1, 7 and 10-14 under 35 U.S.C. § 102(e) as being anticipated by U.S Patent Publication No. 6,693,494 to Fan *("Fan")*. The Applicants respectfully traverse this rejection.

A prior art reference anticipates a claimed invention under 35 U.S.C. § 102 only if every element of the claimed invention is identically shown in that single reference, arranged as they are in the claims. *(MPEP § 2131; In re Bond, 910 F.2d 831, 832, 15 U.S.P.Q.2d 1566, 1567 (Fed. Cir. 1990))*. Anticipation is only shown where each and every limitation of the claimed invention is found in a single prior art reference. *(MPEP § 2131; In re Donahue, 766 F.2d 531, 534, 226 U.S.P.Q. 619, 621 (Fed. Cir. 1985))*.

Fan discloses a phase locked loop (PLL) that includes a phase comparator (PFD), a charge pump, a loop filter and a voltage controlled oscillator (VCO) in the main path, and a fractional-N frequency divider in the return path. In his analysis of *Fan* for the assessment of the novelty of the claimed subject-matter, the Examiner equates the claimed voltage shift capacitor with capacitor C1,

or more probably with capacitor C3, shown in Figure 6 of *Fan*. However, neither C1 nor C3 is a capacitor coupling the phase comparator and the VCO.

In the context of the invention, the expression "a voltage shift capacitor coupling the phase comparator and the voltage controlled oscillator of a phase locked loop" recited in the independent claims means that the voltage shift capacitor, or any capacitive structure comprising such a capacitor, is connected in series between the output of the phase comparator and the input of the voltage controlled oscillator (see e.g., *page 2, lines 14-17 of the description*). The independent claims have been amended to clarify this feature of the invention, whereby reciting that the voltage shift capacitor is a series capacitor.

In contrast, capacitor C3 of *Fan* is connected between the input of the VCO and the ground. Being so connected, capacitor C3 is actually a parallel capacitor, not a series capacitor. Therefore, from a structural standpoint, capacitor C3 of *Fan* cannot be compared with the claimed voltage shift capacitor.

Actually, the circuit of Figure 6 of *Fan* which comprises capacitors C1 and C3 corresponds to the loop filter 22 of the PLL. Such a loop filter is also to be seen, under item 20, on Figures 2 and 6 of the present application, wherein capacitors C2 and C1 and resistor R2 correspond to capacitors C1 and C3 and to resistor R1, respectively, of the loop filter of Figures 2 and 6 of *Fan*. The loop filter of the PLL, nevertheless, is not part of the claimed circuit for charging a voltage shift capacitor of a PLL. It is true that the capacitive elements of the loop filter contribute to the definition of the voltage which controls the VCO, with the consequence that it must be charged or discharged when the frequency of the signal at the output of the VCO must be changed. Nevertheless, the invention is directed to a control circuit for controlling a coupling capacitor placed in series between the phase comparator and the VCO.

Since no such series capacitor is disclosed in *Fan*, the technical teaching in *Fan* is not relevant to the claimed subject-matter. *Fan* admittedly discloses means for charging capacitors upstream of the VCO, namely capacitors belonging to the loop filter. Nevertheless, these means differ from the means recited in the claims both from a functional and from a structural standpoint.

From a functional standpoint, first, they are not convenient for charging a capacitor placed in series. The capacitor which these means are adapted to charge, namely capacitor C3 of the loop filter 22, is a parallel capacitor. Therefore, the teaching disclosed in *Fan* cannot be used to achieve the technical result which is sought by the invention.

From a structural standpoint, further, the means for charging disclosed in *Fan* fail to specifically comprise an input intended to be coupled with the output of the phase comparator and an output intended to be coupled with the input of the voltage controlled oscillator, by which input and output they can be placed in parallel with a series voltage shift capacitor coupling said phase comparator and said voltage controlled oscillator, as recited in the independent claims.

In the Office Action, the Examiner points generally at the input of the charge pump and at the output of the loop filter, which, indeed, are coupled to the output of the PFD and to the input of the VCO, respectively. It is respectfully submitted, however, that this statement of the Examiner merely amounts to an analysis through insight, in the sense that the Examiner identifies nodes in the PLL which would only artificially correspond to the input and the output recited in the claims.

It is the applicant's view that the Examiner has failed to show that these nodes qualify as input and output of a functional entity which could in any way correspond to the claimed circuit. Indeed, the functional entity which is defined by the independent claims as being a voltage shift control circuit comprises three types of means, namely controlled charging means, controlled pre-charging means and controlled polarization means, which are arranged in a certain way so as to ensure given functionalities when the circuit is placed in parallel with a capacitor through its input and its output. As there is no series capacitor in *Fan*, what is disclosed in *Fan* cannot be regarded as a functional entity which would provide these functionalities at such a capacitor.

To conclude, even if one could isolate the means 62, 63, 64, 65, Sb and Sc of the loop filter 22 of *Fan* from the rest of the elements which are present between the output of the PFD and the input of the VCO of *Fan* and name them, according to the Examiner's analysis of *Fan*, a "voltage shift control circuit", it would remain the following differences:

- these means of *Fan* which the Examiner wrongly identifies with the controlled charging means and controlled pre-charging means of the invention are comprised in the loop filter 22 of *Fan*, which is not at all a circuit adapted for being placed in parallel with a series voltage shift capacitor, but rather a circuit connected in parallel between the node defined by the input of the VCO and the ground;
- these means 62, 63, 64, 65, Sb and Sc of *Fan* do not provide the feature of the claimed controlled polarization means. The Examiner refers to the 1-bit quantizer 40 shown in Figure 4 of *Fan*, which is comprised in the low pass filter 29 of Figure 3 of *Fan*. However, there is absolutely no disclosure in *Fan* to support the Examiner's statement that *Fan* teaches that the 1-bit quantizer allows to ensure the polarization of the input of the voltage shift control circuit (identified with the output of the PFD by the Examiner). *Fan* only discloses (see paragraph [0032] of *Fan*) that the 1-bit quantizer allows to speed-up the discharging of the capacitor C of the low pass filter 29.

For the above reasons, the Office Action has not shown that *Fan* anticipates the Applicant's invention as recited in Claims 1, 7 and 10-14. Accordingly, the Applicants respectfully request withdrawal of the § 102 rejection and full allowance of Claims 1, 7 and 10-14.

Rejection under 35 U.S.C. § 103 (Obviousness)

Claims 2-5, 8 and 9 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,693,494 to *Fan* in view of U.S. Patent No. 6,611,161 to *Kumar et al.* This rejection is respectfully traversed.

Indeed, Claims 2-5, 8 and 9 are dependent claims that depend directly or indirectly on independent claims which are deemed allowable for the reasons set forth above. Therefore, they are likewise allowable based on at least the same reasons and based on the recitations contained in each dependent claim.

Conclusion

Given the above amendments and accompanying remarks, the independent claims are believed to be in condition for allowance. The dependent claims that depend directly or indirectly on these independent claims are likewise allowable based on at least the same reasons and based on the recitations contained in each dependent claim.

If the undersigned attorney has overlooked a teaching in any of the cited references that is relevant to the allowability of the claims, the Examiner is requested to specifically point out where such teaching may be found. Further, if there are any informalities or questions that can be addressed via telephone, the Examiner is encouraged to contact the undersigned attorney at (312) 263-4700.

Reconsideration and allowance of the foregoing claims are respectfully requested.

Respectfully submitted,

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